WHAT IS CLAIMED IS:

1. A method for reducing clock skew in an integrated circuit having a plurality of circuit blocks, the method comprising:

providing a first source clock coupled to a clock input terminal of a first circuit block within the circuit blocks;

providing a second source clock coupled to a clock input terminal of a second circuit block within the circuit blocks; and

switching the clock input terminal of the second circuit block to the first source clock when the second circuit block is configured to operate in synchronization with the first circuit block, thereby operating the first and second circuit blocks in accordance with the same first source clock.

2. The method of claim 1 further comprising:

providing an operation mode signal; and

setting a first state to the operation mode signal, thereby operating the second circuit block in synchronization with the first circuit block.

3. The method of claim 2 further comprising:

setting a second state to the operation mode signal, wherein the second circuit block operates asynchronously to the first circuit block when the operation mode signal is at the second state; and

switching the clock input terminal of the second circuit block to the second source clock, thereby

independently operating the first circuit block in accordance with the first source clock and the second circuit block in accordance with the second source clock.

4. An apparatus for reducing clock skew in an integrated circuit having a plurality of circuit blocks, comprising:

a first multiplexer, an output terminal of the first multiplexer coupled to a clock input terminal of a first circuit block within the circuit blocks, a first input terminal of the first multiplexer coupled to a first source clock, and a second input terminal of the first multiplexer coupled together to the first input terminal of the first multiplexer, wherein a selection terminal of the first multiplexer receives an operation mode signal; and

a second multiplexer, an output terminal of the second multiplexer coupled to a clock input terminal of a second circuit block within the circuit blocks, a first input terminal of the second multiplexer coupled to the first source clock, and a second input terminal of the second multiplexer coupled to a second source clock, wherein a selection terminal of the second multiplexer receives the operation mode signal;

wherein the first and the second multiplexers have substantially the same architecture, such that a signal of the first source clock, propagated by the first and the second multiplexers respectively, has substantially the same delay.

5. An apparatus for reducing clock skew in an integrated circuit having a plurality of circuit blocks, comprising:

a first multiplexer, an output terminal of the first multiplexer coupled to a clock input terminal of a first circuit block within the circuit blocks, a first input terminal of the first multiplexer coupled to a first source clock, and a second input terminal of the first multiplexer coupled together to the first input terminal of the first multiplexer, wherein a selection terminal of the first multiplexer receives an operation mode signal;

a second multiplexer, an output terminal of the second multiplexer coupled to a clock input terminal of a second circuit block within the circuit blocks, a first input terminal of the second multiplexer coupled to the first source clock, and a second input terminal of the second multiplexer coupled to a second source clock, wherein a selection terminal of the second multiplexer receives the operation mode signal; and

a control circuit, an output terminal of the control circuit coupled to the selection terminal of the first multiplexer and the selection terminal of the second multiplexer, to provide the operation mode signal on the output terminal of the control circuit;

wherein the first and the second multiplexers have substantially the same architecture, such that a signal of the first source clock, propagated by the first and the second multiplexers respectively, has substantially the same delay.

6. The apparatus of claim 5, wherein the control circuit outputs the operation mode signal in response to a setting of a basic input/output system (BIOS).

7. The apparatus of claim 5, wherein the control circuit is constructed of a jumper.